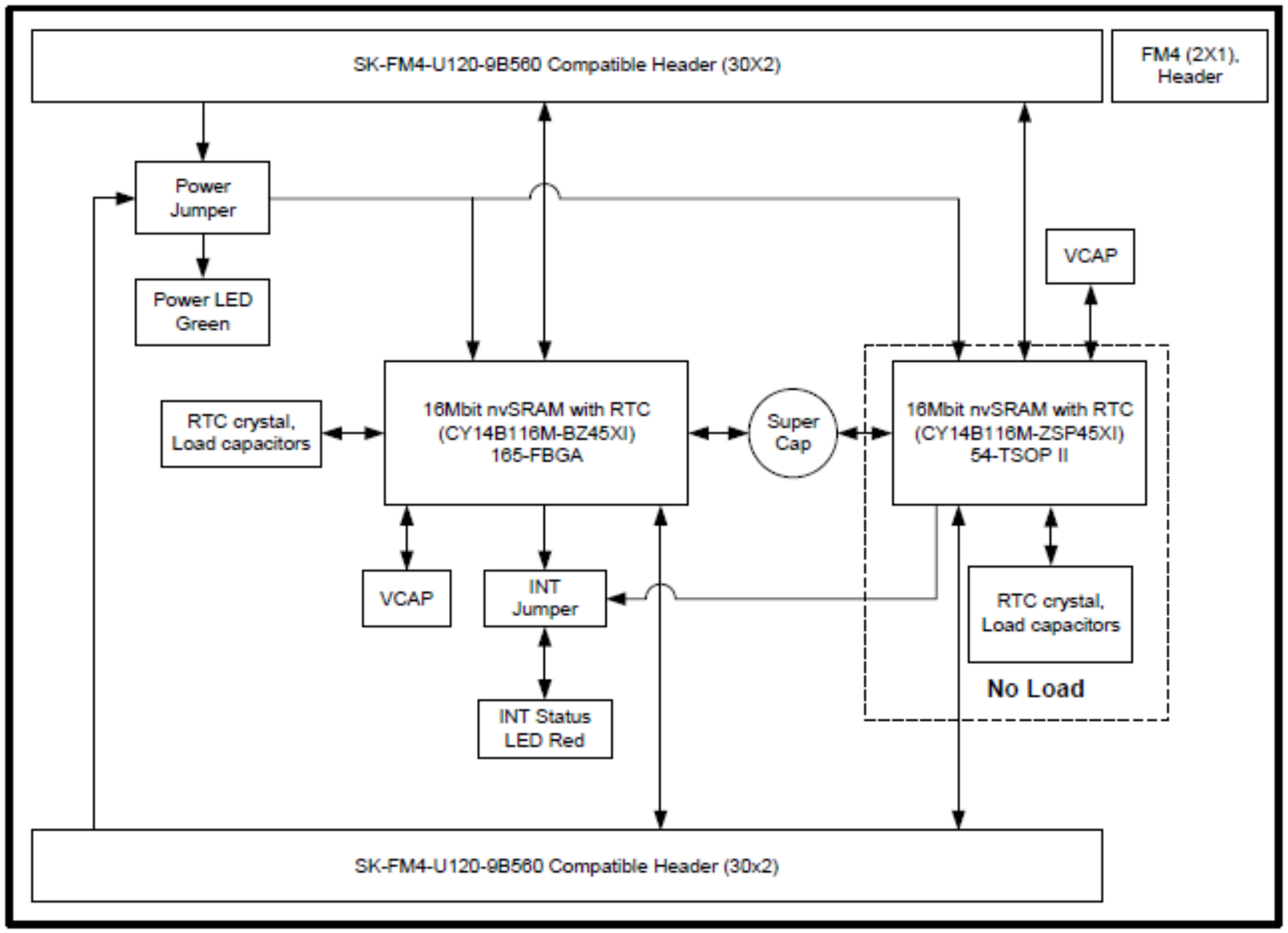
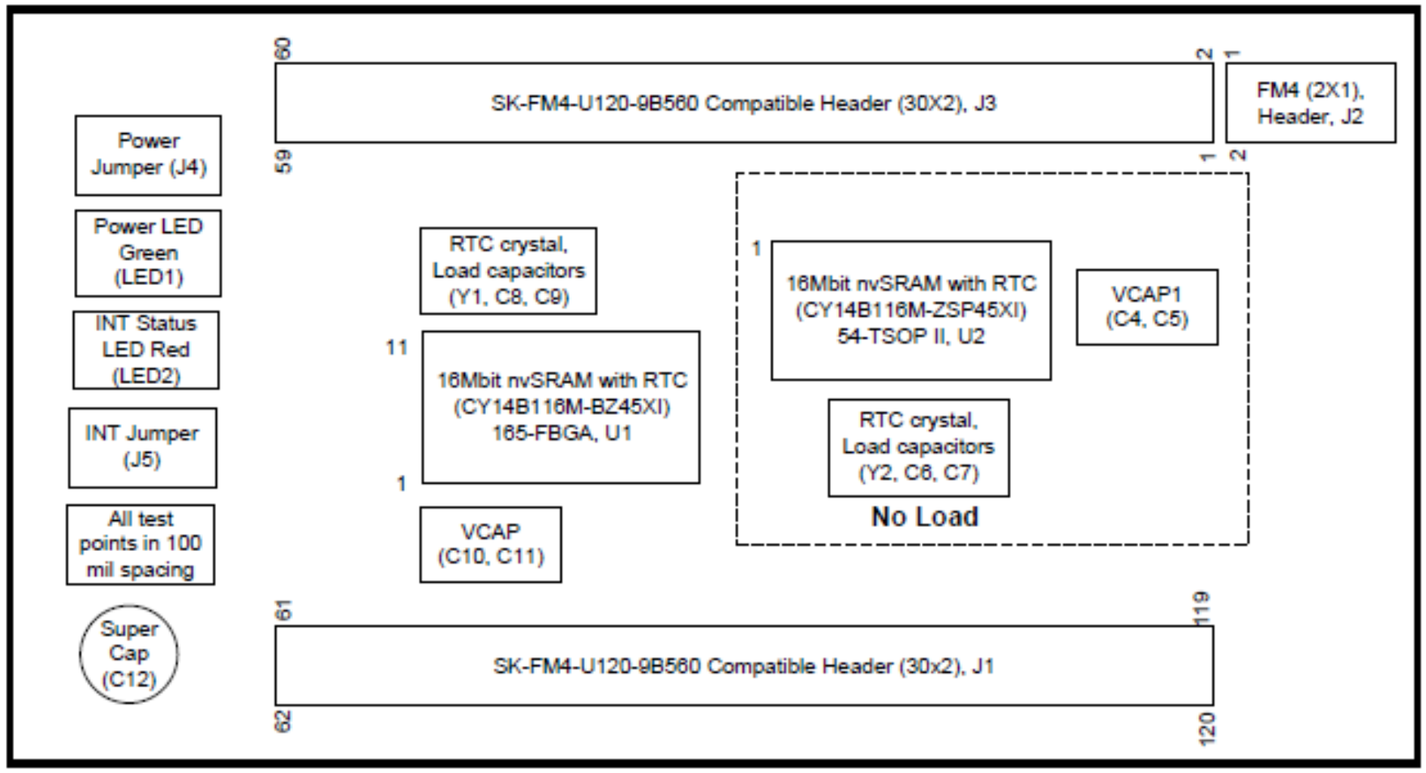


Block Diagram

PCA: 121-60231-01
PCB: 600-60263-01
FAB DRW: 610-60257-01
ASSY DRW: 620-60265-01

CYPRESS SEMICONDUCTOR © 2015		
Title: CY14NVSRAMKIT-001 nvSRAM Development Kit		
Size: A4	Document Number: 630-60263-01	Rev: 01
Date: Wednesday, October 28, 2015	Sheet 1 of 5	



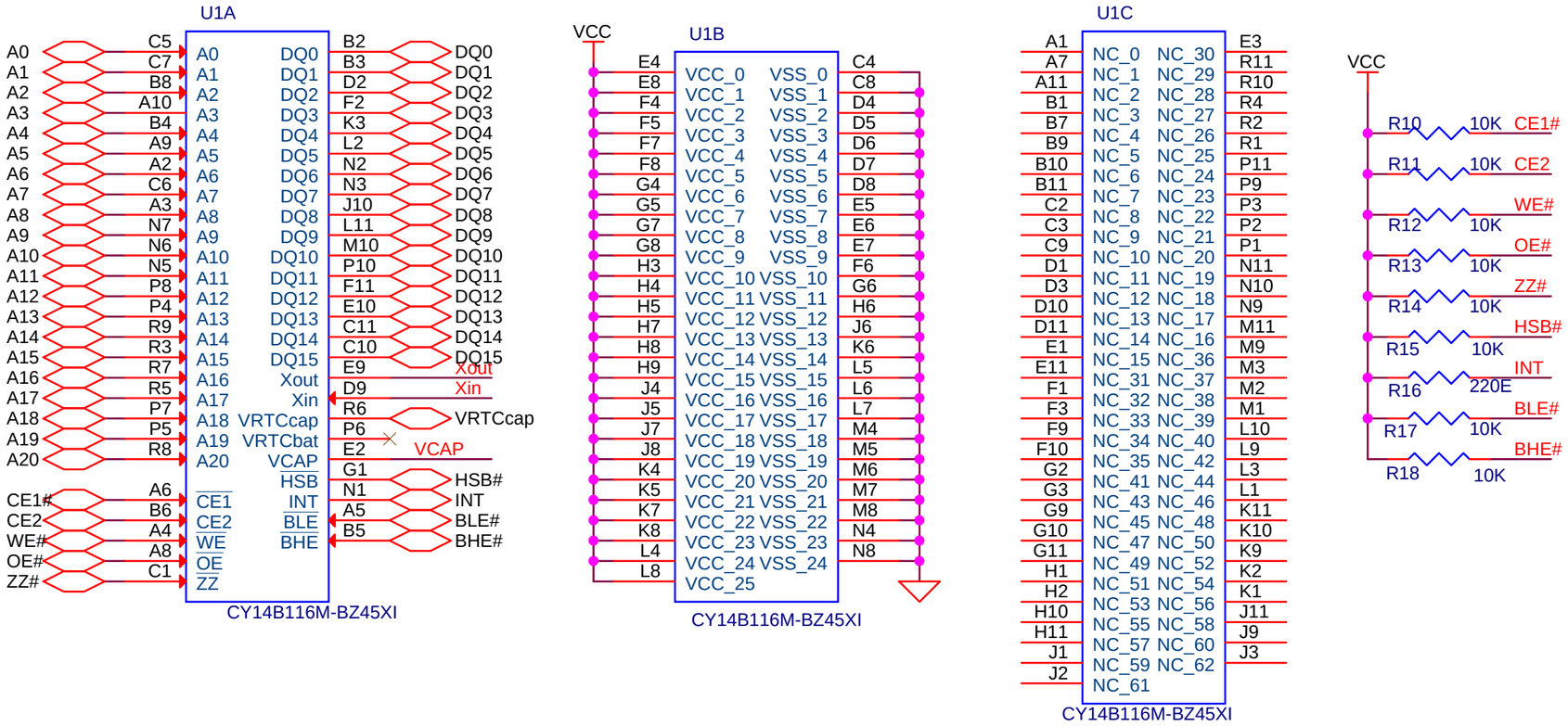
Board Placement Diagram

PCA: 121-60231-01
PCB: 600-60263-01
FAB DRW: 610-60257-01
ASSY DRW: 620-60265-01

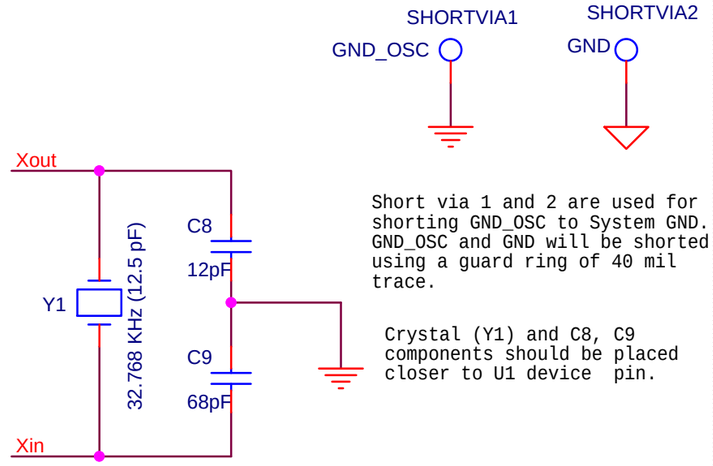
CYPRESS SEMICONDUCTOR © 2015

Title: **CY14NVSRAMKIT-001 nvSRAM Development Kit**		
Size: A4	Document Number: **630-60263-01**	Rev: **01**
Date: Wednesday, October 28, 2015	Sheet 2 of 5	

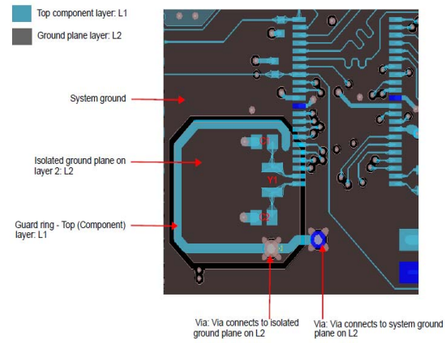
nvSRAM 165 FBGA IC1

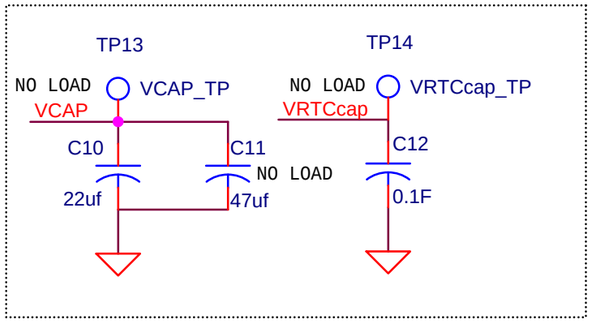


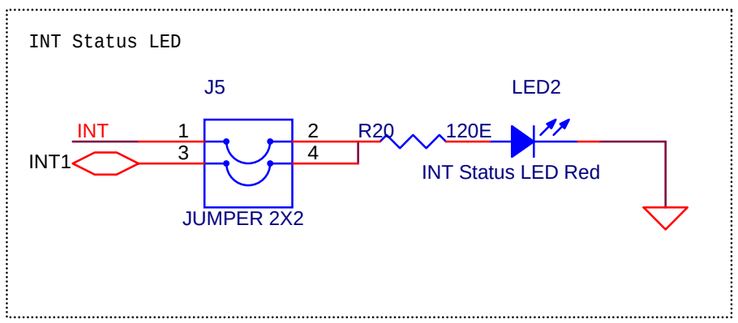
External RTC Components

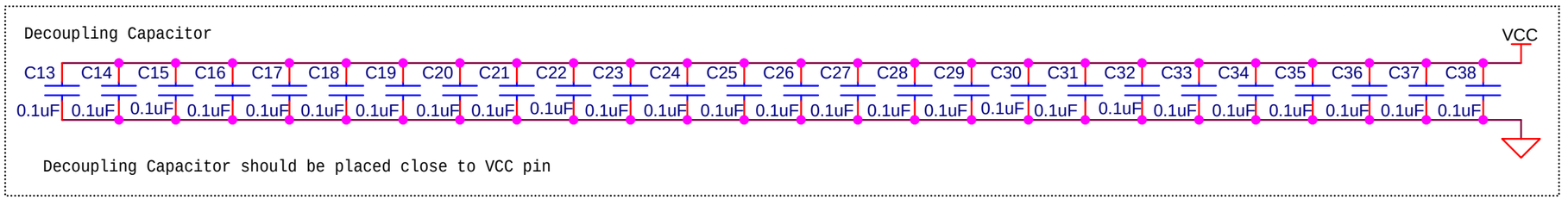


RTC reference Layout







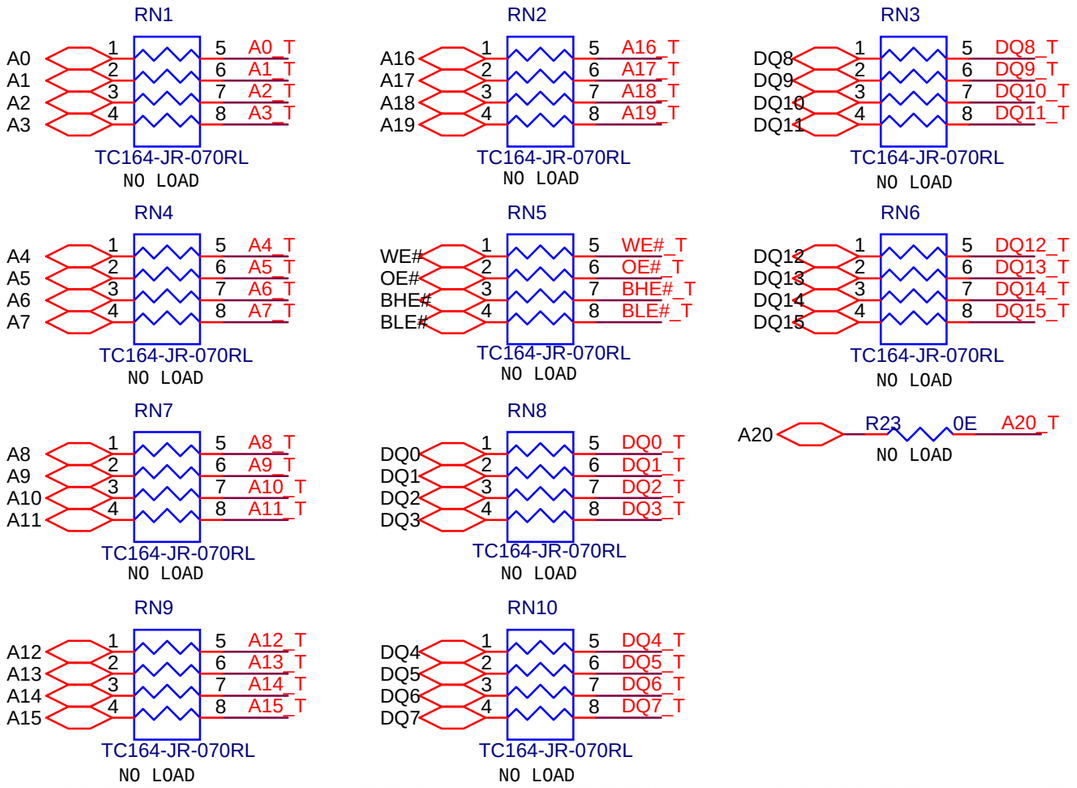


PCA: 121-60231-01
PCB: 600-60263-01
FAB DRW: 610-60257-01
ASSY DRW: 620-60265-01

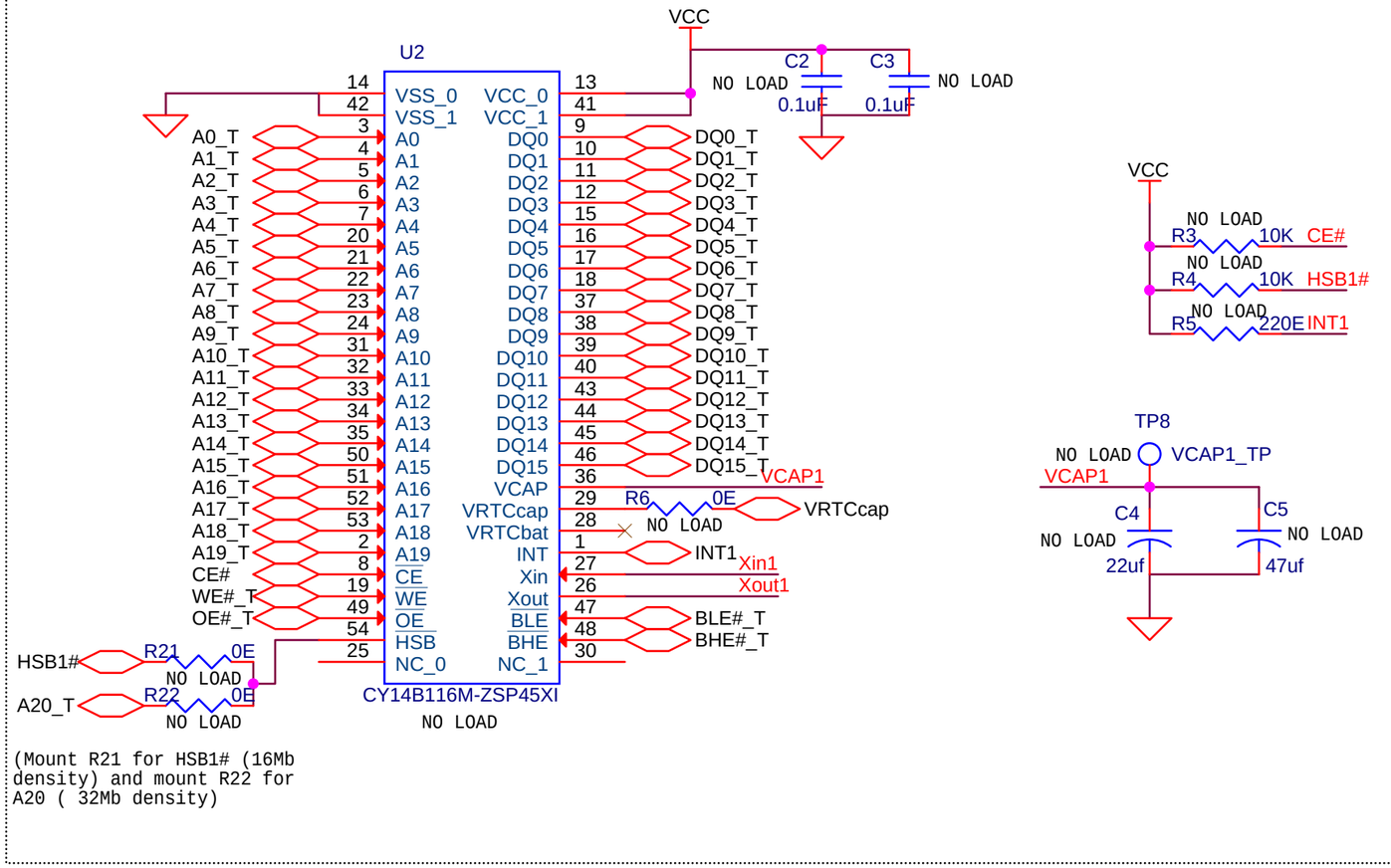
CYPRESS SEMICONDUCTOR © 2015

Title	CY14NVSRAMKIT-001 nvSRAM Development Kit	
Size: A4	Document Number: 630-60263-01	Rev: 01
Date: Monday, November 16, 2015	Sheet 3 of 5	

0 ohm Series resistor between IC1 and IC2 to isolate signals



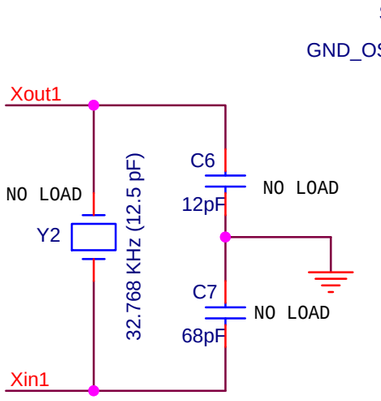
nvSRAM 54 TSOP II IC2

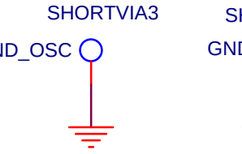


(Mount R21 for HSB1# (16Mb density) and mount R22 for A20 (32Mb density)

External RTC Components

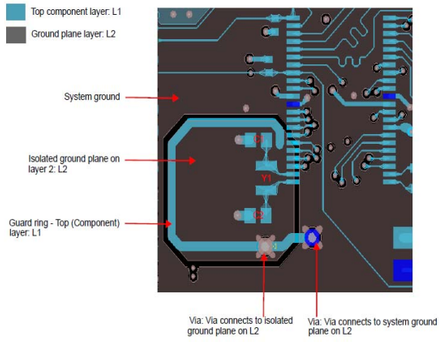
Crystal (Y2) and C6, C7 components should be placed closer to U2 device pin.





Short via 3 and 4 are used for shorting GND_OSC to System GND. GND_OSC and GND will be shorted using a guard ring of 40 mil trace.

RTC reference Layout



PCA: 121-60231-01
PCB: 600-60263-01
FAB DRW: 610-60257-01
ASSY DRW: 620-60265-01

CYPRESS SEMICONDUCTOR © 2015

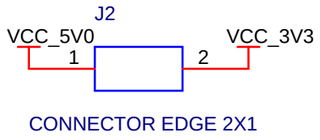
Title: **CY14NVSRAMKIT-001 nvSRAM Development Kit**

Size	Document Number	Rev
A4	**630-60263-01**	**01**

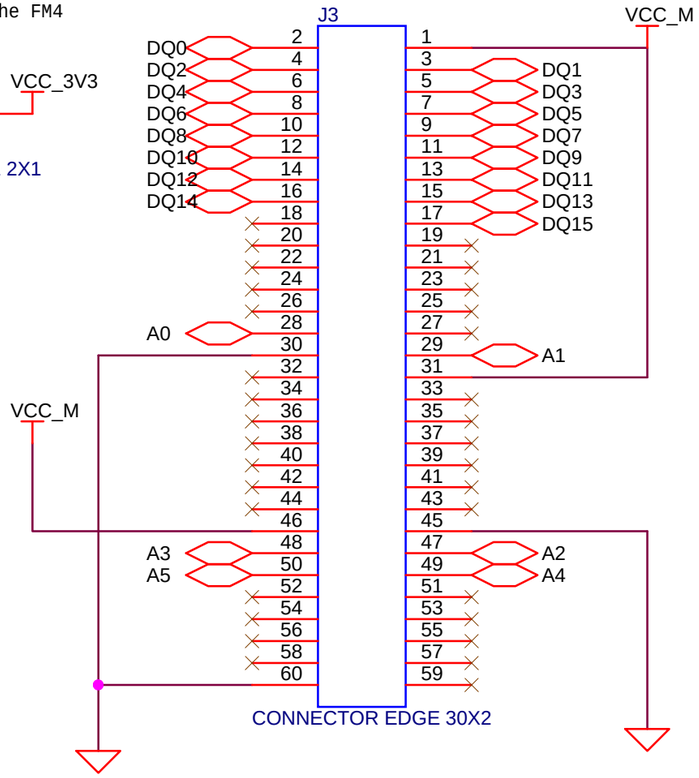
Date: Monday, November 16, 2015 Sheet 4 of 5

Plug in connector to FM4 board

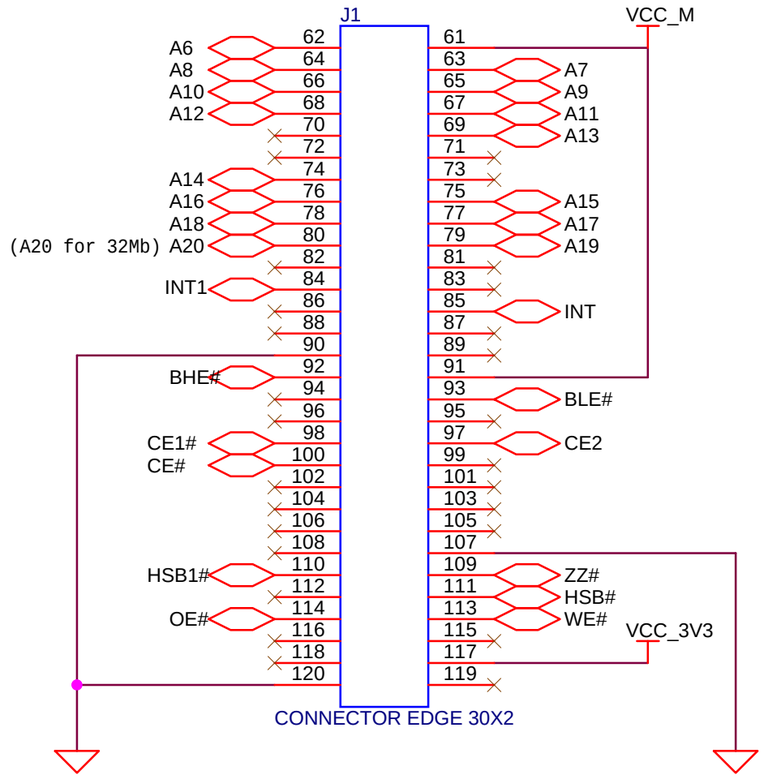
J5 placement should be aligned with J16 on the FM4 board



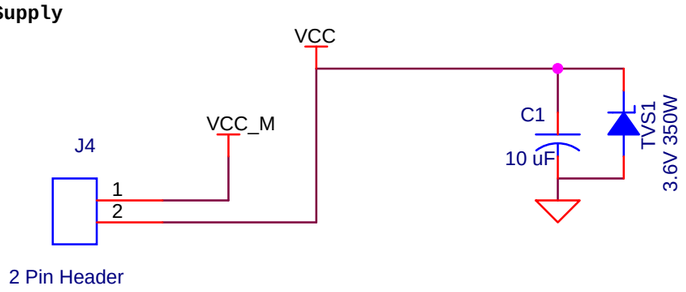
J3 CONNECTS TO U2-1 AND U2-2 (1 TO 60 PIN) OF FM4 BOARD

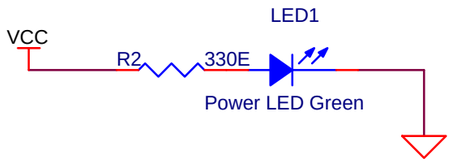


J1 CONNECTS TO U2-3 AND U2-4 (61 TO 120 PIN) OF FM4 BOARD

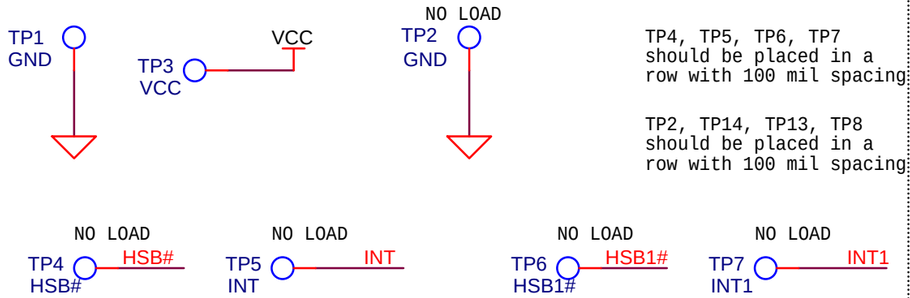


Power Supply





Test Points



PCA: 121-60231-01
PCB: 600-60263-01
FAB DRW: 610-60257-01
ASSY DRW: 620-60265-01

CYPRESS SEMICONDUCTOR © 2015

Title: **CY14NVSRAMKIT-001 nvSRAM Development Kit**

Size	Document Number	Rev
A4	**630-60263-01**	**01**

Date: Thursday, November 05, 2015 Sheet 5 of 5